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By: Vera Ponnsoni Date: 9/30/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Wolfgang Werner

Applic. No. : 09/931,689

Filed : August 16, 2001

Title : IGBT With PN Insulation and Production Method

Examiner : Dana Farahani

Group Art Unit : 2814

RESPONSE

Hon. Commissioner of Patents and Trademarks,
Washington, D. C. 20231

Sir :

Responsive to the Office action dated June 28, 2002, the following remarks are made:

Remarks:

Applicants (hereinafter, Applicant) hereby request reconsideration of the application.

Applicant acknowledges the Examiner's confirmation of receipt of the claim for priority and certified copy of the priority application under 35 U.S.C. § 119(a)-(d).

Claims 1-6 are now in the application.

In item 2 on page 2 of the Office action, claims 1-4 have been rejected as being obvious over Japanese patent JP05082775 under 35 U.S.C. § 103.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the reference.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for an IGBT with PN insulation, comprising:

a low-doped semiconductor substrate of a first conductivity type;

*a low-doped drift zone of the first conductivity type formed in said low-doped semiconductor substrate;*

*a first highly doped well zone of the first conductivity type and a second highly doped well zone of a second conductivity type, opposite to the first conductivity type, successively disposed between said drift zone and said semiconductor substrate.*

The *present invention* is directed to an insulated gate bipolar transistor (IGBT) having a weakly doped drift zone of a first conductivity type formed in a weakly doped semiconductor substrate of the same conductivity type. A highly doped first well zone of the first conductivity type and a highly doped second well zone of a second conductivity type are disposed between the drift zone and the semiconductor substrate.

Accordingly, the IGBT is embedded with an n-cathode 5, a p-base zone 4, an $n^-$-drift region 2 and a p-anode zone 6 in a "double well". The double well has a first $n^+$-well zone 8 and a second $p^+$-well zone 9. The two well zones are provided in an $n^-$-semiconductor body 1. See Fig. 1.

The two well zones 8, 9 and the semiconductor body 1 can be connected by a short-circuit strap 10 or 11. See claims 3-4 of the instant application. Further, the anode zone 6 can be embodied annularly. See claim 2 of the instant application. The IGBT of the *present invention* is a lateral component, since the double well completely surrounds the IGBT cell 3.

The reference numerals corresponding to the above-features are presented solely for illustrative purposes. They are not intended to narrow the scope of the claims for any reason whatsoever.

The JP 05082775 reference discloses a semiconductor device with an $n^+$-source zone 17, a first p-base zone 23, a second p-base zone 25, an n-floating emitter zone 24, an $n^+$-base layer 14, an n-base layer 13 and a $p^+$-anode zone 12. The zones are disposed in a vertical configuration. See Fig. 1, JP 05082775. In other words, the emitter terminal E is located on a first side of the semiconductor device, and the anode terminal is provided on a second side which is opposite the first side.

Thus, the n-floating emitter zones 24 and the first p-base zone 23 are *not* well zones that surround an IGBT cell (in contrast to claim 1 of the instant application).

Nevertheless, even if the zones 23, 24 are considered to be well zones in a substrate 10 (formed by the regions 12, 13, 14), an IGBT cell is not present within the well zones 23, 24. This is so because the regions provided within the well zone 24 (i.e., the $n^+$-source zone 17 and the second p-base zone 25) do not form such a cell.

In addition, in JP 05082775, a gate electrode 26 is provided above the zones 23, 24. The gate electrode 26 is separated from the zones by an insulation layer (indicated by the channels 35, 36, 37). Thus, the well zones are not connected with each other by a short-circuit strap. The same also holds true for the substrate 10, since the gate electrode 26 is located at a distance from the substrate 10 (or from the region 14) on an insulation layer 18. See Fig. 3, JP 05082775.

Applicant further submits that, if the n-floating emitter zone 24 of JP 05082775 is compared with the drift zone 2 of the *present invention*, it can be seen that JP 05082775 is missing the anode zone that surrounds the cell 17, 25 at a distance (on the edge of the zone 24).

Clearly, the reference does not show "*a low-doped drift zone of the first conductivity type formed in said low-doped semiconductor substrate; a first highly doped well zone of the*

*first conductivity type and a second highly doped well zone of a second conductivity type, opposite to the first conductivity type, successively disposed between said drift zone and said semiconductor substrate*", as recited in claim 1 of the instant application (emphasis added). Thus, neither can the specific combination of the aforementioned limitations be shown.

Applicant further believes that there is no teaching or suggestion in the reference indicating such modifications, as asserted by the Examiner.

In other words, the features including the limitations "*a low-doped drift zone of the first conductivity type formed in said low-doped semiconductor substrate; a first highly doped well zone of the first conductivity type and a second highly doped well zone of a second conductivity type, opposite to the first conductivity type, successively disposed between said drift zone and said semiconductor substrate*", as recited in claim 1, attain the present invention's objectives and are <u>not taught or suggested</u> by the reference, whether taken alone or in any combination (emphasis added).

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since

all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-6 are solicited.

In item 2 of the Office action, the Examiner has presented a discussion of product-by-process claims. The Examiner has also stated that "in claims 5 and 6, the method of making IGBT is given no patentable weight". Counsel is quite astounded by this comment since claims 5 and 6 are method claims. Of course, method claims have method limitations and of course they have patentable weight.

In the event the Examiner should still find any of the claims to be unpatentable, the Examiner is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and

Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

VRP:cgm

September 30, 2002

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